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The Data Acquisition System for the KOTO Detector

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Abstract

The Data Acquisition (DAQ) for the KOTO detector is designed around a 14-bit 125MHz ADC module, which measures the energy and the time of photomultiplier pulses from about 4000 readout channels. The Trigger has a two-tiered design, with a first level decision based on the time-aligned energy sum over the entire calorimeter and a second level decision based on clustering and in-time veto signal rejection. Data accepted by the second level trigger are read out via Gigabit Ethernet and passed to a computer farm for event building and data storage.

Keywords: DAQ; trigger; KOTO

1. Introduction

The goal of the KOTO experiment [1] at the Japan Proton Accelerator Research Complex (J-PARC) is to discover and measure the rate of the rare decay of the neutral K_L meson into a neutral

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pion, a neutrino and an antineutrino ($K_L^0 \to \pi^0 \nu\bar{\nu}$). The Standard Model predicts a branching ratio of $(2.43 \pm 0.39 \pm 0.06) \times 10^{-11}$[2]. The experiment is a follow-up to E391a at KEK[3], with a completely redesigned beam line, a new Cesium Iodide (CsI) calorimeter with increased granularity and reduced shower leakage, and a new digitization, trigger and data acquisition system. In the following we will review the experimental technique and the physics considerations used in the design of the KOTO DAQ.

Using the same experimental methods pioneered by E391a, KOT0 aims at detecting the two photons from the π^0 decay using a high acceptance, finely segmented CsI calorimeter contained in a vacuum pressure vessel. The K_L are generated by 30 GeV protons hitting a nickel or platinum target and extracted in spills of 0.7 s duration every 3.3 s. A carefully crafted beam line, placed at a 16^o angle with respect to the proton direction, produces a highly collimated K_L beam with a rectangular shape of 7.8 μsr solid angle.

Figure 1 contains a transverse view of the KOT0 detector along the direction of the K_L beam, which defines the detector *z*-axis. The CsI calorimeter is surrounded by a hermetic veto of photon (FB, MB, BHPV) and charged particle detectors (BCV, CV and BHCV); a set of collar counters (CC01 to CC06) surrounds the beam at different positions along *z*. The ensemble of these veto detectors are able to identify single neutral and charged particles with less than 10^{-4} inefficiency[4], thus rejecting K_L decays with multiple π^0's or with a single π^0 plus charged pions or electrons in the final state. Using the measured position of the two photons at the calorimeter front face and the constraint $(x,y)=(0,0)$ for the K_L decay vertex, one can fully reconstruct the K_L decay kinematics with the extra assumption that the two photons come from a π^0. The analysis is done requiring that signal events fall in a 2-dimensional region of the K_L decay *z*-vertex and its transverse momentum p_T. This provides additional rejection against events with only two photons in the final state such as $K_L^0 \to \gamma\gamma$ or $\eta^0 \to \gamma\gamma$. The best present limits on this K_L rare decay come from a direct measurement performed by KEK E391a, $BR(K_L^0 \to \pi^0 \nu\bar{\nu}) \le 2.6 \times 10^{-8}$ [3] at the 90% confidence level (CL), and from the measured $K^+ \to \pi^+ \nu\bar{\nu}$ branching ratio [5], using the Grossman-Nir bound, $BR(K_L^0 \to \pi^0 \nu\bar{\nu}) \le 1.5 \times 10^{-9}$.

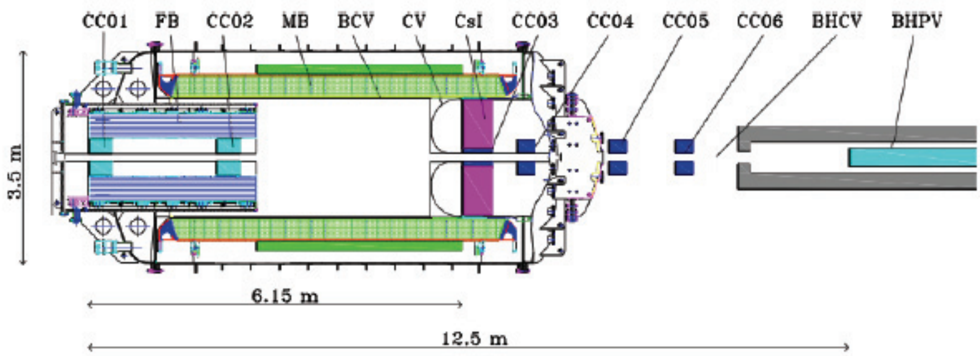

Figure 1: Schematic transverse view of the KOTO detector. The K_L beam enters the centre of the pressure vessel from the left in the figure.

The physics requirements on the DAQ are as follows: 1 MeV sensitivity for photons with 1.5 GeV maximum energy deposition which, assuming 10 count/MeV, translates into 14 bit dynamic range for energy measurements in the calorimeter; sub nanosecond timing resolution to resolve physics events with on-time extra particle production from accidental superimposition of $K_L^0 \rightarrow \pi^0 \nu\bar{\nu}$ with photons and neutron decays from the beam halo; and a pipelined frontend and trigger electronics to minimize the dead time generated by the DAQ system.

These requirements are accomplished via a frontend 125 MHz ADC board and a two-level trigger system. Data accepted by the second level trigger are read out via Gigabit Ethernet into a computer cluster through a 48-port network switch. A single Master Control and Trigger Supervisor (MACTRIS) module supervises the integration of frontend, trigger, readout and external accelerator signals. Control signals generated by MACTRIS are multiplied and distributed by a FANOUT module. Figure 2 shows a pictorial overview of the electronics designed for the KOTO DAQ. Two different sizes 21-slots VME crates are used in the system: up to sixteen 6U VME64x crates for the ADC boards; and three 9U VIPA crates, with a custom designed P3 backplane besides the standard P1 and P2 backplanes, for the TRIGGER and FANOUT boards. The DAQ modularity is such that each frontend crate, populated with up to 16 ADC boards, receives control from a single FANOUT module and sends data to a single L1 and L2 TRIGGER board.

In Sections 2 through 4 of this paper we will review the design of the frontend board (KOTO ADC Module), of the boards generating and distributing the DAQ control signals (MACTRIS and FANOUT) and of the board responsible for signal event trigger and readout (TRIGGER Module), respectively. Section 5 details the parameters of the readout computer farm (Mandolin).

2. The KOTO ADC Module

A single frontend ADC board [6] has been designed to receive photomultiplier (PMT) signals from approximately 3000 CsI calorimeter channels and about 1000 channels of upstream, downstream and beam hole veto detectors. The ADC board injects the analog differential inputs from up to 16 channels into a 10-pole Gaussian/Bessel low pass filter before digitization. The 10-pole filter is designed to produce a quasi gaussian pulse with about 45 ns full width at height maximum. The shaped signal is digitized by a 14-bit 125 MHz flash ADC chip. A simultaneous measurement of both the charge and the time of the hit with respect to a global starting time t_0 is obtained by fitting for the height and the position of the peak of the digitized gaussian shape, respectively.

The digitized shaped pulses are stored inside a 4 μsec deep pipeline while waiting for the trigger decision. The sum over the 16 channels is sent via a 2.5 GBPS optical link to the first level trigger electronics, which compares the time aligned energy sum over the whole calorimeter to a programmable threshold. Upon a first level trigger decision, the data are buffered to a second level trigger electronics via a second 2.5 GBPS optical link.

The ADC board exchanges four control signals, three inputs and one output, with the rest of the DAQ. The inputs are a 8 ns system clock (CLK); a gate for the length of the spill duration (LIVE), whose initial edge provide the t_0 for the whole system; and a level 1 trigger accept signal (L1A). The output is a signal indicating that the board is not self-detecting any error condition (ERROR).

The pulse shaping circuit on the 125 MHz FADC board is optimized depending on whether it receives analog signals from the calorimeter or from the veto detectors. The harsh background conditions for event with a photon escaping through the beam hole in the center of the calorimeter required the development of a 4-channel 500 MHz version of the ADC board for the readout of forward beam veto counters [7].

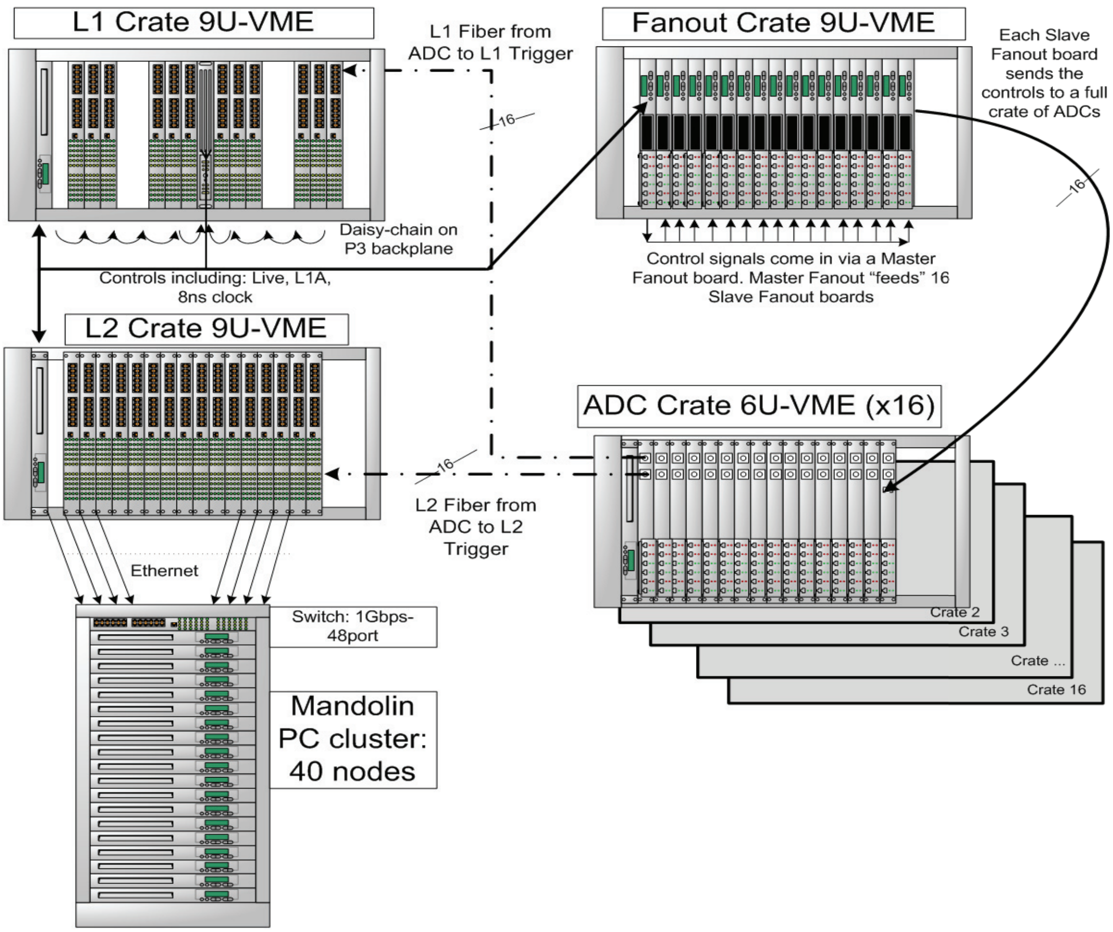

Figure 2: Schematic view of the KOTO detector DAQ electronics.

3. The MACTRIS and FANOUT Modules

MACTRIS is a 9U VME board designed to supervise the integration of frontend, trigger, readout and external accelerator signals. It is located in a specific slot of the L1 Trigger Crate for reasons discussed below. It generates the 8 ns system clock via an on-board quartz oscillator and distributes it to each board in the KOTO DAQ in LVDS differential format. Two distribution solutions are available: a “front panel” solution using a repeater FANOUT boards with controlled length routing and CAT6a cables; and a “backplane” solution, in which the clock is picked up by individual boards on reserved P2 backplane lines. The first distribution system is used to generate copies of the clock to each frontend ADC board. The second solution is used to distribute the clock to the L1 and L2 Trigger boards.

MACTRIS is also responsible for generating and distributing the LIVE gate for the duration of the spill. The start and length of this gate is determined by NIM signals received from the accelerator. Finally, MACTRIS is designed to calculate the final total calorimeter energy and compare it to a programmable energy in order to generate a L1A decision. Energy sums from the two halves of the calorimeter are obtained by connecting the L1 TRIGGER boards in daisy chain fashion via the custom designed P3 backplane. The two daisy chains start on the outermost slots and connect adjacent boards from the outside in. MACTRIS is designed to tap into the P3 backplane pins of the crate middle slot, where the two daisy chains end. The LIVE and L1A signals are distributed as differential LVDS signals using the same solutions described for the system clock. While the front panel solution is limited to four signals, with the logical OR of all of the ERROR signals received by each ADC being the fourth signal, the backplane solutions allows for up to 34 DAQ control signals being exchanged between MACTRIS and the TRIGGER boards. These signals are used to control the second level trigger decision and the orderly transmission of data to the backend readout.

The FANOUT module is a 1-to-16 repeater board for the four control signals using the front panel distribution solution. A first module, identified as Master FANOUT, is directly connected to MACTRIS and makes a copy of the control signals to be distributed to sixteen Slave FANOUT modules, which in turn distribute these signals to each ADC board in the system.

4. The TRIGGER Module

The L1 and L2 TRIGGER boards are 9U custom designed modules housed in two separate crates. Although each board has very distinct functionalities, they share the same board design and layout. In the following paragraph, a general description of the board features is given. The rest of the section details the different use of the common layout.

Each TRIGGER board is designed to receive sixteen 2.5 GBPS optical links; each link is deserialized in a Texas Instrument TLK3101 chip and sent as a 16-bit wide bus to a XC5VFX70 Xilinx FPGA. This Virtex 5 FPGA is also connected to VME signal and DAQ Controls pins of the P1 and P2 VME backplane, as well as to the total energy daisy-chain pins of the P3 backplane. A dedicated 32-bit wide data bus and 8-bit wide address bus directly connect the Virtex 5 FPGA to a second XC4VFX12 Xilinx FPGA. This Virtex 4 FPGA has connections to two 2Gb DDR2 memories and to a front panel 1Gb Ethernet port.

The L1 TRIGGER module is responsible for receiving the energy sum from sixteen ADC boards and generating a time aligned local sum of its sixteen inputs plus the daisy-chain partial energy sum from the adjacent L1 TRIGGER. A dedicated sync word is used to mark the beginning of fiber data transmission after each LIVE so that internal delays between different input fibers and between different L1 TRIGGER boards in the daisy chain can be calibrated at the beginning of each spill.

The L2 TRIGGER modules is responsible for receiving 16 channel worth of triggered data from each fiber link and buffering it in 16K deep FIFOs, before being stored in one of the two 2Gb memories for the 0.7 s duration of the spill. By “event” here we refer to the fixed number of digitized samples, typically 32 to 64, which have to be collected for each trigger in order to fit the gaussian shaped signals after the Bessel filter. At the same time, the other memory is being read out via the

Gigabit port for the 3.3 s period between spills. This two memory solution eases one of the bottlenecks of the KOTO DAQ: the read out via a single 1GBPS output of sixteen 2.5 GBPS inputs. L1 trigger rates of 14 kHz can thus be reached for events with 48 digitized samples.

5. The Readout Farm

Data accepted by the L2 TRIGGER board are read out via Gigabit Ethernet and passed to a 41-node computer cluster called Mandolin. Here event reconstruction and filtering, data monitoring and temporary data storage take place. Each node consists of a Dell PowerEdge SC1435 server with two dual-core AMD Opteron 2.6 GHz processors, 16 GB RAM memory, a 250 GB system disk plus a 750 GB data disk. Each node also comes with two embedded 1-Gb Network Interface Controllers, one of which is dedicated to receive the data from the L2 TRIGGER boards.

To maximize the read out speed, event fragments from different fiber links are arranged into Jumbo Ethernet packets and sent out the L2 TRIGGER board via User Datagram Protocol (UDP). Each packet contains the energy of sixteen ADC channels for the triggered event plus a header with the event timestamp and encoding for the location of the frontend electronics. Events are sent out simultaneously by all L2 TRIGGER boards and in the same order in which they are triggered.

The full detector readout requires a total of sixteen L2 TRIGGER boards, with each board reporting only a slice of the total event. In order to do event building, slices relative to the same event from different boards have to be routed to the same node as shown in Fig. 4. The routing is done through a 6200 Dell Power Connect Layer 3 network switch with 48 1Gb-ports. This high density switch has up to 184 Gb/s capacity and comes with four additional 10Gb ports. Event slices from 16 consecutive triggers are routed to 16 separate nodes. Each node is responsible for data integrity checking and event building using the packet header information. Data reduction using veto rejection and data compression eases the second bottleneck in the KOTO DAQ caused by the limited speed of data writing to disk. The data are eventually saved in a multi TB disk array capable of receiving data from the switch using the 10Gb Ethernet port.

Conclusions

The design for the DAQ of the KOTO experiment is presented. A pipelined frontend and trigger electronics is designed to efficiently identify events with two photons in the final states at rates up to 14 kHz. The readout is based on Gigabit Ethernet via a high speed commercial switch. Event fragments are routed to a single node of a computer farm for event reconstruction before final storage. The first KOTO physics run is planned for winter 2013.

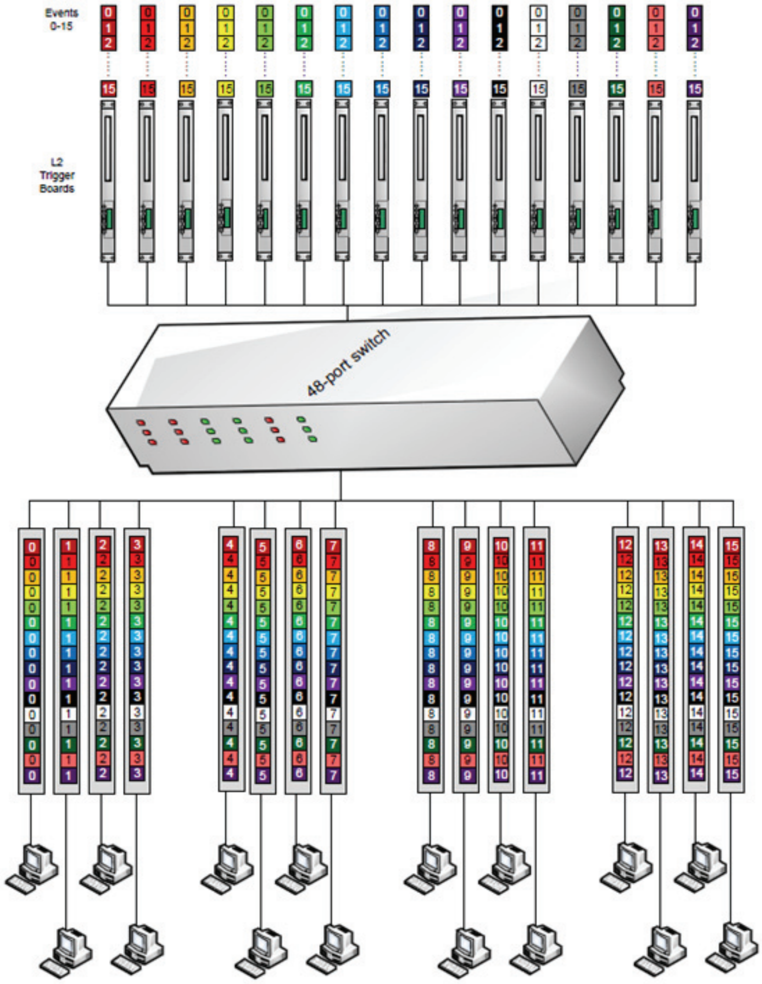

Figure 4: Cartoon of the KOTO readout structure: events slices from consecutive triggers, represented as squares of same color and increasing number, are directed to a single Mandolin node via the 48-port switch.

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